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(54) **Sense amplifier circuit for semiconductor memory devices**

Leseverstärkerschaltung für Halbleiterspeicheranordnungen

Circuit amplificateur de détection pour dispositifs de mémoire à semi-conducteurs

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Description

[0001] The present invention relates to a sense amplifier circuit for semiconductor memory devices. More specifically, this invention relates to a sense amplifier circuit particularly adapted to Flash EEPROM devices.

[0002] It is known that a semiconductor memory device comprises a matrix ("memory matrix") of memory cells located at the intersections of rows and columns of the matrix. The rows of the matrix are normally called "word lines", and the columns of the matrix are called "bit lines".

[0003] A Flash EEPROM memory cell is comprised of a floating gate MOS field effect transistor with drain and source electrodes, a control gate electrode and a floating gate electrode; the control gate electrode is connected to a respective word line of the memory matrix, the drain electrode is connected to a respective bit line, and the source electrode is connected to a reference potential.

[0004] The Flash EEPROM memory cell can be electrically programmed (or "written") and erased; during writing, electrons are transferred into the floating gate electrode of the floating gate MOSFET by means of the so-called Channel Hot Electron ("CHE") effect; during erasing, electrons are removed from the floating gate electrode by means of Fowler-Nordheim tunneling.

[0005] The presence of electron charges on the floating gate electrode modifies the current/voltage characteristic of the floating gate MOSFET. In fact, the threshold voltage of the floating gate MOSFET varies according to the charge on its floating gate electrode: a written memory cell has a threshold voltage higher than that of an erased memory cell.

[0006] This difference in threshold voltages is exploited during reading mode to determine if a particular memory cell is erased or written: the word line to which the control gate electrode of the memory cell to be read is connected is raised to a voltage between the threshold voltage of an erased memory cell and that of a written memory cell, and the voltage of the bit line to which the drain electrode of the memory cell is connected is also raised. In these conditions, if the memory cell to be read is a written memory cell it will not sink current (because the voltage on the control gate electrode of the memory cell is lower than its threshold voltage), while if it is an erased memory cell it will sink current (because the voltage on its control gate electrode is higher than its threshold voltage).

[0007] Known sense amplifier circuits substantially comprise current/voltage converters which convert the current sunk by the memory cell to be read in a voltage signal. Typically, this voltage signal is compared with a reference voltage signal obtained by current/voltage conversion of a reference current; the reference current is the current sunk by a so-called "reference memory cell", which is a floating gate MOSFET identical to those constituting the real memory cells but having a predetermined threshold voltage, corresponding to the so-called "virgin state" (the condition achieved by a floating gate MOSFET after it has been submitted to Ultra-Violet light). In this way, all the spurios effects, such as statistical geometrical and process variations between memory cells, voltage variations, and so on, are eliminated, because they are trated as common-mode signals.

[0008] A specific problem of Flash EEPROM devices is related to the fact that Flash EEPROM devices are not erased on a per-byte basis, but on a per-sector basis. This means that many memory cells (from thousand to millions) are simultaneously submitted to electrical erasing. Consequently, it is not possible to individually control the behaviour of each memory cell during erasing, the only feasible thing being a statistical approach. Slight differences in the electric characteritics of the conductive paths between the memory cells and the voltage rails, as well as in the geometry of the memory cells, determine a statistical distribution of the erasing time of the memory cells, and cause after erasing a dispersion of values of memory cells' electric parameters such as the threshold voltage, the memory cell current and so on. Therefore, after repeated electrical writing and erasing cycles, some of the floating gate MOSFETs may happen to be overerased to the extent that their threshold voltages (normally positive) become negative.

[0009] The existence of even only one depleted memory cell leads to the failure of the whole memory device. Infact, a depleted memory cell sinks a finite current even when it is not selected (i.e. when the voltage on its control gate electrode is zero); when an attempt is made to read a written memory cell belonging to the same bit Line as the depleted memory cell, the current sunk by the latter causes the sense amplifier circuit to erroneously read the written memory cell as an erased memory cell. In other words, the current sunk by a depleted memory cell can be regarded as an offset current which adds up to the current sunk by the memory cell to be read; this offset current causes an offset voltage to be superimposed on the output voltage signal of the current/voltage converter. The offset voltage, if large enough, can be responsible for the incorrect reading of a written memory cell as an erased memory cell.

[0010] The patent application EP 505 915 discloses a static type random access memory device that is equipped with sense amplifier circuits (141 to 14n) for rapidly developing small differential voltage levels respectively indicative of data bits read out from selected memory cells (MC11 to MCmn) to digit line pairs (DL1 to DLn), and the input nodes (N16/ N17) of each sense amplifier circuit are coupled with the associated digit line pair through a pair of capacitors (CPa/ CPb), wherein the digit line pairs and the input nodes are respectively precharged to a high voltage level (Vdd) and an intermediate voltage level (Vdd/2) so that the sense amplifier circuits start on developing immediately after activation thereof.

[0011] In view of the state of the art described, an ob-

ject of the present invention is to provide a new sense amplifier circuit for semiconductor memory devices in general, and particularly adapted to Flash EEPROM devices in that it is not affected by the presence of depleted memory cells.

[0012] According to the present invention, such an object is achieved by means of a sense amplifier circuit for a semiconductor memory device according to claim 1.

[0013] The sense amplifier circuit according to the present invention is not affected by the presence of an offset current, such as that introduced by a depleted memory cell in a Flash EEPROM device, at least as long as such an offset current does not take very high values. In fact, thanks to the provision of said capacitive means between the current-to-voltage converted signal and the comparator, any offset in the converted voltage signal is decoupled from the comparator's input being DC contribute; only the fluctuations of the converted voltage signal, corresponding to the current sunk by the memory cell to be read, with respect to such a DC contribute are fed to the comparator.

[0014] The features and advantages of the present invention will be made more evident by the following detailed description of two particular embodiments, illustrated as non-limiting examples in the annexed drawings, wherein:

Figure 1 is a schematic electric diagram of a sense amplifier circuit according to a first embodiment of the present invention;
Figure 2 is a schematic electric diagram of an address transition detection circuit for the control of the sense amplifier circuit of Figure 1;
Figures 3A to 3D are timing diagrams of some signals of the sense amplifier circuit of Figure 1;
Figure 4 is a schematic electric diagram of a sense amplifier circuit according to a second embodiment of the present invention;
Figure 5 is a schematic electric diagram of an address transition detection circuit for the control of the sense amplifier circuit of Figure 4;
Figure 6A to 6G are timing diagrams of some signals of the sense amplifier circuit of Figure 4 and of the address transition detection circuit of Figure 5.

[0015] As shown in Figure 1, a sense amplifier circuit according to a first embodiment of the present invention substantially comprises two current/voltage converter branches 1, 2 and a comparator 3.

[0016] A first current/voltage converter branch 1, also called "matrix branch", is coupled to a group of bit lines BL of a matrix of memory cells MC of a semiconductor memory device. In the case of a Flash EEPROM device, each memory cell is represented by a floating gate MOSFET with a drain electrode connected to one respective bit line BL of the matrix, a source electrode commonly connected to the source electrodes of all the other memory cells, and a control gate electrode connected to one respective word line WL of the matrix. The memory cells MC belonging to the bit lines BL which are coupled to the same current/voltage converter branch 1 form a memory portion reserved to an external data line of the memory device (Flash EEPROM devices generally comprise eight or sixteen external data lines).

[0017] According to a known arrangement, the bit lines BL coupled to the same current/voltage converter branch 1 are grouped in packets 4, for example eight, each packet 4 comprising for example eight bit lines BL. Inside each packet 4, each bit line BL is connected to a source electrode of a respective first-level selection N-channel MOSFET 5; drain electrodes of all the first-level selection MOSFETs 5 inside each packet 4 are commonly connected to a source electrode of a respective second-level selection N-channel MOSFET 6; drain electrodes of all the second-level selection MOSFET 6 are commonly connected to a node 7 of the first current/voltage converter branch 1.

[0018] A gate electrode of each MOSFET 5 is connected to a respective first-level bit line selecion signal YN0-YN7; similarly, a gate electrode of each MOSFET 6 is connected to a respective second-level bit Line selection signal or packet selection signal YM0-YM7. Signals YN0-YN7 and YM0-YM7 are generated in a per-se known way by an address decoding circuitry 50 (schematically shown in Figure 2) supplied with external address signals A0-An of the memory device. Such address decoding circuitry also generates word line selection signals WL0,WL1,...WLm for the selection of the word lines WL.

[0019] An N-channel MOSFET 8 (typically of the so-called "native" kind, that is a transistor having a much lower threshold voltage than an "enhancement" transistor: typically, the threshold voltage of an enhancement transistor is about 1 V, and that of a native transistor is 0.4-0.5 V) has a source electrode connected to node 7, a drain electrode connected to a node 9 of the first branch 1, and a gate electrode connected to an output of an inverter 10 whose input is connected to node 7. A P-channel MOSFET 11 has a drain electrode connected to node 8, a source electrode connected to a voltage supply Line VDD, and a gate electrode connected to node 9. MOSFET 8 and inverter 10 form a so-called "drain voltage regulator" for the memory cells MC, and keep the voltage at node 7 at a value of about 1 V, to prevent soft writing of the memory cells MC during reading.

[0020] Node 9 is connected to one plate of a capacitor C1, whose second plate is connected to a node 12 to which a drain electrode of a P-channel MOSFET 13 is also connected; MOSFET 13 has a source electrode connected to the voltage supply line VDD, and a gate electrode connected to an output of an inverter 14 whose input is connected to a signal ATD ("Address Transition Detected"), activated by an address transition detection circuit (shown in Figure 2) upon recognition of a change in the external address signals of the memory

device, as it will be better explained later on. Node 12 is also connected to one input of the comparator 3.

[0021] The second current/voltage converter branch 2 is substantially similar to the first branch 1. Branch 2 is coupled to a so-called "reference" bit line BLR made up of "reference" memory cells MCR; the reference memory cells MCR are totally similar to the memory cells MC, except for the fact that their threshold voltages are set to the value of an UV erased memory cell.

[0022] The reference bit line BLR is connected to a node 15 of the second branch 2 through two serially-connected N-channel MOSFETs 16, 17 whose gate electrodes are both connected to the voltage supply line VDD; these two MOSFETs 16, 17 simulate the effect of the first- and second-level selection MOSFETs 5 and 6 in series to each bit line BL on the first branch 1, in order to have, as far as possible, identical electrical paths between the voltage supply line VDD and the memory cells MC and MCR, respectively.

[0023] The reference memory cells MCR can be immersed in the matrix of memory cells MC. In alternative, the reference memory cells MCR can be immersed in a little matrix of reference memory cells external to the matrix of memory cells MC.

[0024] Similarly to node 7 in the first branch 1, node 15 is connected to a drain voltage regulator comprising an N-channel MOSFET 18 (native kind) and an inverter 19. A drain electrode of MOSFET 18 is connected to a node 20 of the second branch 2 to which a drain electrode of a P-channel MOSFET 21 is also connected; MOSFET 21 has a source electrode connected to the voltage supply line VDD, and a gate electrode connected to node 20. A capacitor C2 has one plate connected to node 20, and a second plate connected to a node 22 to which a drain electrode of a P-channel MOSFET 23 is also connected; MOSFET 23 has a source electrode connected to VDD and a gate electrode connected to the output of the inverter 13. Node 22 is further connected to a second input of the comparator 3.

[0025] An output 24 of the comparator 3 is supplied to a latch 25, whose output 26 is supplied to an output buffer (per-se known and therefore not shown) which drives a respective external data line (also not shown).

[0026] As shown in Figure 2, the Flash EEPROM device is also provided with an address transition detection circuit. Each external address signal A0-An supplies directly a first input of a XNOR (exclusive NOR) logic gate 27 and, through a delay line D, a second input of the XNOR gate 27. The outputs of all the XNOR gates 27 are commonly connected and supplied to an input of a monostable circuit 28; the output of the monostable circuit 28 forms the signal ATD.

[0027] Upon a Logic state transition of even only one of the external address signals A0-An, a pulse of a predetermined duration is produced at the output of the monostable circuit 28.

[0028] Figures 3A-3D show the temporal succession of event in a read operation of a written memory cell and of an erased memory cell.

[0029] A read operation starts when the logic configuration of the external address signals A0-An changes; at the instant t0 one (YNi) of the first-level selection signals YN0-YN7 and one (YMj) of the second-level selection signals YM0-YM7 are activated by the address decoding circuitry 50 (Fig. 3A); which one of the signals YN0-YN7 and YM0-YM7 is actually activated depends on the particular Logic configuration of the external address signals A0-An. One of the first-level selection MOSFETs 5 and one of the second-level selection MOSFETs 6 are turned on, so that the bit Line BL which contains the memory cell to be read is connected to the node 7 of the current/voltage converter branch 1. The reference bit line BLR is instead permanently connected to node 15 of the second converter branch 2.

[0030] Since none of the word line selection signals WL0-WLm is activated, no current will flow in the second converter branch 2 the voltage V20 at node 20 and V22 at node 22 is therefore equal to VDD. If no depleted (i. e. negative threshold voltage) memory cells are present in the selected bit line BL, the first converter branch 1 will be run through by a transient current, until a parasitic capacitance CBL of the selected bit line BL is charged to the voltage set by the drain voltage regulator 8 and 10; as the parasitic capacitance CBL is charged, the voltage V9 at node 9 and V12 at node 12 raises towards VDD.

[0031] As long as MOSFETs 13 and 23 are off, nodes 12 and 22 are floating, being only connected to the high-impedance inputs of the comparator 3.

[0032] Differently, if one or more of the memory cells MC of the selected bit line BL are depleted, the depleted memory cells sink a finite current even if their gate voltage is zero; consequently, even after the parasitic capacitance CBL of the bit line has been charged, a current will continue to flow in the first converter branch 1: such a current can be regarded as an offset current which causes the voltage V9 to set at a value lower than VDD, due to the voltage drop across MOSFET 11; the difference between VDD and the actual voltage V9 is an offset voltage. In conventional sense amplifier circuits, such an offset current could be responsible, if sufficiently high, for an erroneous reading of a written memory cell for an erased memory cell.

[0033] The change in the address signals A0-An also produces, at an instant t1 (Fig. 3B), the generation of an address transition detection pulse in the signal ATD. The ATD pulse turns the P-channel MOSFETs 13 and 23 on, to connect nodes 12 and 22 to VDD. If no depleted memory cells are present in the selected bit line BL, capacitor C1 charges to a voltage VC1 equal to zero. If instead the selected bit line BL contains depleted memory cells, capacitor C1 will charge to a voltage VC1 equal to the difference between the voltage V12 at node 12 (VDD) and the voltage V9, this last depending on the offset current introduced by the depleted memory cells. The ATD pulse has a predetermined duration at Least sufficient

to assure that capacitor C1 is completely charged. Capacitor C2 charges to a voltage VC2 substantially equal to zero, since both its plates are at VDD.

[0034] When the ATD pulse ends, MOSFETs 13 and 23 turn off, and nodes 12 and 22 are disconnected from VDD (they are left substantially floating, since they are connected to the inputs of the comparator 3).

[0035] At an instant t2, after the end of the ATD pulse, the address decoding circuitry 50 activates one (WLk) of the word line selection signals WL0,WL1...WLn (Fig. 3C); the voltage of the selected word line WL is raised to VDD. One of the reference memory cells MCR of the reference bit line BLR is turned on and starts sinking current: this causes a drop in the voltage at node 20; since no discharge paths exist for capacitor C2, the voltage V22 at node 22 follows the voltage V20, and sets to a value determined by the dimensional ratio between MOSFET 21 and the reference memory cell MCR (Fig. 3D).

[0036] Since it is supposed that the memory cell MC connected to the selected bit line BL and word line WL is a written memory cell, the voltage VDD on its control gate electrode is not sufficient to turn it on, and it will not sink current; the voltage V9 does not vary, and also the voltage V12 substantially remains at the VDD level. The voltage V12 is higher than the voltage at node 22; this voltage difference is detected by comparator 3, whose output 24 switches to, for example, the "0" logic level; this logic level is stored in the latch 25 which drives the respective external data line (typically by means of an output buffer circuit) to deliver the read datum.

[0037] Let's suppose now that at an instant t4 the logic configuration of the external addreass signals A0-An changes, to start a new read operation. The word Line selection signal WLk is disactivated. At an instant t5 one (YNi',YMj') of the first- and second-level selection signals YN0-YN7 and YM0-YM7 are activated, to connect a new bit line BL to the converter branch 1; at an instant t6 the ATD pulse starts, and at an instant t7, successive to the end of the ATD pulse, one (WLk') of the word line selection signals WL0,WL1...WLm is activated to select a new word line.

[0038] Since it is supposed that the memory cell MC connected to the selected bit line BL and word line BL is now an erased memory cell, the voltage VDD on its control gate electrode turns it on, and the cell sinks current; this current adds to the offset current introduced by the depleted memory cells (if they are present) and causes a further drop in the voltage V9; since capacitor C2 has no discharge paths, the voltage V12 follows the voltage V9, and drops below the voltage V22 (because the current sunk by an erased memory cell MC is higher than that sunk by the UV-erased reference memory cell MCR). The output 24 of the comparator 3 switches to the "1" logic level, and this logic level is stored in the Latch 25.

[0039] Capacitor C1 decouples node 12 from node 9. During the ATD pulse, capacitor C1 is charged to a voltage VC1 which compensates the offset voltage introduced in the first converter branch 1 by any offset current of depleted memory cells. Thus, the voltage V12 is the same as if no depleted memory cells were present.

[0040] It is important to note that for a correct working of the sense amplifier circuit previously described it is necessary not to have an overlap between the ATD pulse and the word line selection signal WL0,WL1,... WLm. In fact, it is necessary for capacitor C1 to be charged to a voltage VC1 compensating the voltage drop produced at node 9 by the offset current only; the ATD pulse must be long enough to assure that capacitor C1 is completely charged.

[0041] The latch 25 is necessary to prevent spurious transitions of the external data line caused by the slow discharge of capacitor C1 by means of leakage currents.

[0042] Those skilled in the art will surely recognize that the speed performances of the previously described sense amplifier circuit, as well as of the amplifier circuit according to the known art, are mainly limited by the Long settling time of V20 due to the slow discharge of a parasitic capacitor CBLR associated to the reference bit line BLR.

[0043] Figure 4 shows an alternative embodiment of a sense amplifier circuit according to the present invention, having improved speed performances. In this embodiment, the reference bit line BLR of reference memory cells MCR has been replaced by a single memory cell MCR external to the matrix of memory cells MC. The external reference memory cell MCR is driven by a signal VGR which has a different timing with respect to the word Line selection signals WL0,WL1...WLm (Figures 6C and 6E). Also, P-channel MOSFETs 13 and 23 are controlled by two distinct address transition detection signals ATDM and ATDR with a different timing, as visibile in Figures 6B and 6D.

[0044] This arrangement allows a reduction in the time required to carry on a sensing operation. In fact, having replaced the reference bit line BLR with a single reference memory cell MCR, the time necessary to the voltage V20 to stabilize is lower, since the parasitic capacitance associated to the reference memory cell MCR is much lower than that of CBLR in the previous embodiment. Furthermore, the reference memory cell MCR is now activated before the activation of one (WLk) of the word line selection signals WL0,WL1-WLm, so that when the memory cell to be read is activated the voltage V22 is already settled; this further reduces the time required for sensing a memory cell.

[0045] Figure 5 shows a schematic diagram of an address transition detection circuit for the sense amplifier circuit according to this second embodiment.

[0046] The ATD signal supplies a latch 29, whose output forms the signal ATDR driving the MOSFET 23 of the second converter branch 2. The latch 29 is also supplied with a reset signal R which, at the end of each reading, resets the content of the latch 29. Also, the output of latch 29 is commonly supplied as a first input to a

number of two-inputs AND gates 30 whose second inputs are supplied with a respective one of the word line selection signals generated by the address decoding circuitry 50, and whose outputs form the signals WL0-WLm. The signal ATDR is further supplied to a delay circuit 31 whose output forms the gate signal VGR driving the reference memory cell MCR; the output of the delay circuit 31 is also commonly supplied as a first input to a plurality of two-inputs AND gates 32 whose second inputs are supplied with a respective one of the first- and second-level column selection signals generated by the address decoding circuitry 50, and whose outputs form the signals YN0-YN7, YM0-YM7. The signal VGR is further supplied to a monostable circuit 33 whose output forms the signal ATOM driving the MOSFET 13 of the first converter branch 1.

[0047] As in the circuit of Figure 2, the ATD signal is generated by a transition in at least one of the external address signals A0-An. The activation of the ATD signal (Fig. 6A) causes the activation of the signal ATDR (Fig. 6B), which goes high and remains in this state until the reading of the memory cell has been completed (i.e. until the reset signal R resets it to the low logic state). The signal ATDR, going high, turns the MOSFET 23 off, thus leaving node 22 floating. The signal VGR is activated after a predetermined delay, and goes high (Fig. 6C), thus enabling the signals YNi, YMj to go high (Fig. 6F). Also, the signal VGR starts an ATDM pulse (Fig. 6D) at the output of the monostable circuit, which activates the MOSFET 13 conndecting node 12 to VDD. The length of the ATOM pulse is such that MOSFET 12 turns off before one (WLk) of the signals WL0, WL1,...WLm is activated.

Claims

1. Flash EEPROM memory comprising a sense amplifier circuit comprising first current/voltage conversion means (1) for converting a current of a memory cell (MC) to be read into a voltage signal (V9), second current voltage/conversion means (2) for converting a reference current into a reference voltage signal (V20), and voltage comparator means (3) for comparing said voltage signal (V9) with said reference voltage signal (V20), **characterized by** capacitive decoupling means (C1) for decoupling said voltage signal (V9) from said comparator means (3), and means (13) for providing said capacitive decoupling means (C1) with an electric charge which compensates an offset voltage introduced in said voltage signal (V9) by an offset current superimposed on the current of the memory cell (MC) to be read.

2. Flash EEPROM memory according to claim 1, **characterized in that** said offset current is a current sunk by at least one depleted memory cell (MC) connected in parallel to the memory cell (MC) to be read.

3. Flash EEPROM memory according to claim 1, **characterized in that** said first current/voltage conversion means (1) comprise a first current/voltage coversion branch (1) connected in series between a power supply (VDD) and the memory cell (MC) to be read, said voltage comparator means (3) comprises a comparator (3) with a first input coupled to an output (9) of said first conversion branch (1), and **in that** said capacitive decoupling means (C1) comprise a decoupling capacitor (C1) connected between said first input of the comparator (3) and said output (9) of said first conversion branch (1).

4. Flash EEPROM memory according to claim 3, **characterized in that** said means (13) for providing the capacitive decoupling means (C1) with an electric charge comprise transistor means (13) connected between the first input of the comparator and the power supply (VDD) and activatabLe to electrically connect said capacitor (C1) to the power supply (VDD).

5. Flash EEPROM memory according to claim 4, **characterized in that** said second current/voltage conversion means (2) comprise a second current/voltage conversion branch (2) connected in series between the power supply (VDD) and current generator means generating said reference current, the second converter branch (2) having an output (20) coupled to a second input of the comparator (3).

6. Flash EEPROM memory according to claim 5, **characterized in that** said current generator means comprise a reference memory cell (MCR) identical to the memory cell (MC) to be read and having a predetermined threshold voltage.

7. Flash EEPROM memory according to claim 5 or 6, **characterized by** comprising a second decoupling capacitor (C2) connected between said output (20) of the second converter branch (2) and the second input of the comparator (3), and by comprising second transistor means (23) connected between the second input of the comparator (3) and the power supply (VDD) and activatable to electrically connect the second decoupling capacitor (C2) to the power supply (VDD).

8. Flash EEPROM memory according to claim 7, said semiconductor memory device comprising a matrix of memory cells (MC) located at intersection of rows (WL) and columns (BL) of the matrix, column selection means (5,6) for electrically coupling one of a group of said columns (BL) to said first current/voltage converter branch (1), address decoding means

(50) for generating column selection signals (YN0-YN7,YM0-YM7) for driving said column selection means (5,6) and row selection signals (WL0,WL1,WLm) for selecting one of said rows (WL) in response to external address signals (A0-An) of the memory device, the address decoding means comprises address transition detection means (D,27,28) for temporarily activating said transistor means (13), in response to a change in the external address signals (A0-An), for a predetermined time between the activation of the column selection signals (YN0-YN7,YM0-YM7) and the activation of the row selection signals (WL0,WL1,WLm).

Patentansprüche

1. Flash-EEPROM-Speicher mit einer Leseverstärkerschaltung mit

   einem ersten Strom-/Spannungswandelmittel (1) zum Wandeln eines Stromes einer zu lesenden Speicherzelle (MC) in ein Spannungssignal (V9),
   einem zweiten Strom-/Spannungungswandelmittel (2) zum Wandeln eines Referenzstromes in ein Referenzspannungssignal (V20) und
   einem Spannungsvergleichsmittel (3) zum Vergleichen des Spannungssignales (V9) mit dem Referenzspannungssignal (V20), **gekennzeichnet durch**
   ein kapazitives Entkopplungsmittel (C1) zum Entkoppeln des Spannungssignales (V9) von dem Vergleichsmittel (3) und
   ein Mittel (13) zum Versehen des kapazitiven Entkopplungsmittels (C1) mit einer elektrischen Ladung, die eine OffsetSpannung ausgleicht, die in das Spannungssignal (V9) **durch** einen Offset-Strom eingeführt wird, der dem Strom der zu lesenden Speicherzelle (MC) überlagert ist.

2. Flash-EEPROM-Speicher nach Anspruch 1, **dadurch gekennzeichnet, daß** der Offset-Strom ein Strom ist, der von mindestens einer verarmten Speicherzelle (MC) die parallel zu der zu lesenden Speicherzelle (MC) verbunden ist, abgesaugt wird.

3. Flash-EEPROM-Speicher nach Anspruch 1, **dadurch gekennzeichnet, daß** das erste Strom-/Spannungswandelmittel (1) einen ersten Strom-/Spannungswandelzweig (1) aufweist, der in Reihe zwischen einer Stromversorgung (VDD) und der zu lesenden Speicherzelle (MC) geschaltet ist, wobei das Spannungsvergleichsmittel (3) einen Komparator (3) mit einem ersten Eingang aufweist, der mit einem Ausgang (9) des ersten Wandelzweiges (1) verbunden ist, und daß das kapazitive Entkopplungsmittel (C1) einen Entkopplungskondensator (C1) aufweist, der zwischen dem ersten Eingang des Komporators (3) und dem Ausgang (9) des ersten Wandelzweiges (1) geschaltet ist.

4. Flash-EEPROM-Speicher nach Anspruch 3, **dadurch gekennzeichnet, daß** das Mittel (13) zum Versehen des kapazitiven Entkopplungsmittel (C1) mit einer elektrischen Ladung einen Transistor (13) aufweist, der zwischen den ersten Eingang des Komparators und die Stromversorgung (VDD) geschaltet ist und aktivierbar ist zum elektrischen Verbinden des Kondensators (C1) mit der Stromversorgung (VDD).

5. Flash-EPPROM-Speicher nach Anspruch 4, **dadurch gekennzeichnet, daß** das zweite Strom-/Spannungswandelmittel (2) einen zweiten Strom-/Spannungswandelzweig (2) aufweist, der in Reihe zwischen die Stromversorgung (VDD) und ein Stromgeneratormittel geschaltet ist, das den Referenzstrom erzeugt, wobei der zweite Wandelzweig (2) einen Ausgang (20) aufweist, der mit einem zweiten Eingang des Komparators (3) verbunden ist.

6. Flash-EEPROM-Speicher nach Anspruch 5, **dadurch gekennzeichnet, daß** das Stromgeneratormittel eine Referenzspeicherzelle (MCR) identisch zu der zu lesenden Speicherzelle (MC) aufweist, und mit einer vorbestimmten Schwellenspannung.

7. Flash-EEPROM-Speicher nach Anspruch 5 oder 6, **gekennzeichnet durch** einen zweiten Entkopplungskondensator (C2), der zwischen den Ausgang (20) des zweiten Wandelzweiges (2) und den zweiten Eingang des Komparators (3) geschaltet ist, und **durch** ein zweites Transistormittel (23), das zwischen den zweiten Eingang des Komparators (3) und die Stromversorgung (VDD) geschaltet ist und aktivierbar ist zum elektrischen Verbinden des zweiten Entkopplungskondensators (C2) mit der Stromversorgung (VDD).

8. Flash-EEPROM-Speicher nach Anspruch 7, wobei die Halbleiterspeichervorrichtung eine Matrix aus Speicherzellen (MC), die an Schnittstellen von Zeilen (WL) und Spalten (BL) der Matrix angeordnet sind, ein Spaltenauswahlmittel (5, 6) zum elektrischen Verbinden einer aus einer Gruppe der Spalten (BL) mit dem ersten Strom-/Spannungswandelzweig (1), ein Adressdekodiermittel (50) zum Erzeugen von Spaltenauswahlsignalen (YN0-YN7, YM0-YM7) zum Treiben des Spaltenauswahlmittels (5, 6) und von Zeilenauswahlsignalen (WL0, WL1, WLm) zum Auswählen eine der Zeile (WL) als Re-

aktion auf externe Adreßsignale (A0-An) der Speichervorrichtung aufweist, wobei das Adressdekodiermittel ein Adressübergangserfassungsmittel (D, 27, 28) zum zeitweiligen Aktivieren des Transistormittels (13) als Reaktion auf eine Änderung in den externen Adreßsignalen (A0-An) während einer vorbestimmten Zeit zwischen der Aktivierung der Spaltenauswahlsignale (YN0-YN7, YM0-YM7) und der Aktivierung der Zeilenauswahlsignale (WL0, WL1, WLm) aufweist.

Revendications

1. Mémoire flash EEPROM comprenant un circuit amplificateur de lecture qui comprend des premiers moyens (1) de conversion courant/tension pour convertir un courant d'une cellule de mémoire lue (CM) en un signal de tension (V9), des seconds moyens (2) de conversion courant/tension pour convertir un courant de référence en un signal de tension de référence (V20), et un moyen (3) comparateur de tension pour comparer ledit signal de tension (V9) audit signal de tension de référence (V20), **caractérisée par** des moyens (C1) de découplage capacitif pour découpler ledit signal de tension (V9) dudit moyen comparateur (3), et des moyens (13) pour fournir aux dits moyens (C1) de découplage capacitif une charge électrique qui compense une tension de décalage introduite dans ledit signal de tension (V9) par un courant de décalage qui se superpose au courant de la cellule de mémoire lue (CM).

2. Mémoire flash EEPROM selon la revendication 1, **caractérisée en ce que** ledit courant de décalage est un courant absorbé par au moins une cellule de mémoire (CM) appauvrie, reliée en parallèle à la cellule de mémoire lue (CM).

3. Mémoire flash EEPROM selon la revendication 1, **caractérisée en ce que** lesdits premiers moyens (1) de conversion courant/tension comprennent une première branche (1) de conversion courant/tension, montée en série entre une alimentation (Vdd) et la cellule de mémoire lue (CM), ledit moyen (3) comparateur de tension comprend un comparateur (3) ayant une première entrée reliée à une sortie (9) de ladite branche de conversion (1), et **en ce que** lesdits moyens (C1) de découplage capacitif comprennent un condensateur de découplage (C1) monté entre ladite première entrée du comparateur (3) et ladite sortie (9) de ladite branche de conversion (1).

4. Mémoire flash EEPROM selon la revendication 3, **caractérisée en ce que** lesdits moyens (13) pour fournir une charge électrique aux moyens (C1) de découplage capacitif comprennent un moyen à transistor (13) monté entre la première entrée du comparateur et l'alimentation (Vdd), et activable pour relier électriquement ledit condensateur (C1) à l'alimentation (Vdd).

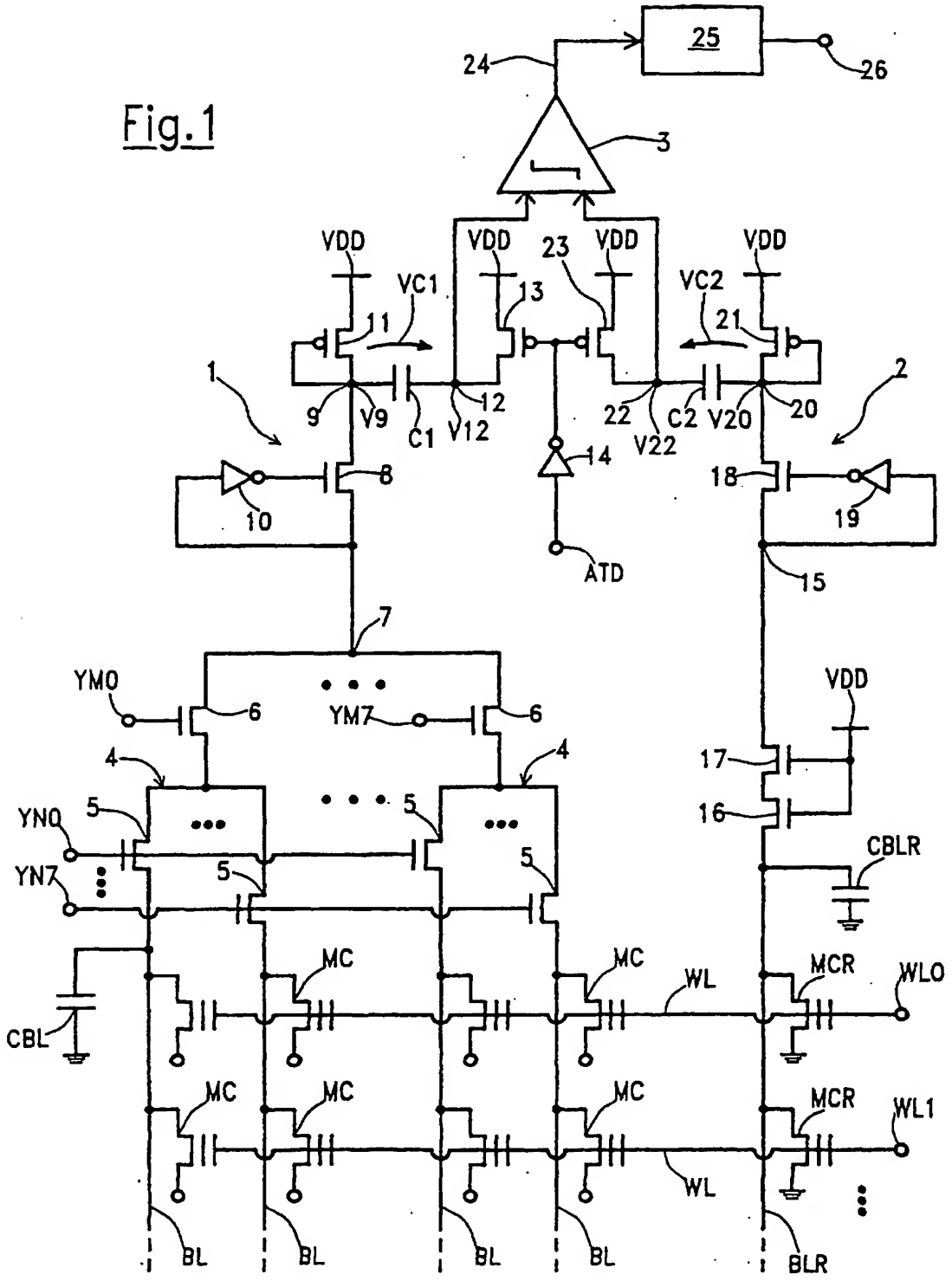
5. Mémoire flash EEPROM selon la revendication 4, **caractérisée en ce que** lesdits seconds moyens (2) de conversion courant/tension comprennent une seconde branche (2) de conversion courant/tension montée en série entre l'alimentation (Vdd) et des moyens générateurs de courant qui génèrent ledit courant de référence, la seconde branche de conversion (2) ayant une sortie (20) reliée à une seconde entrée du comparateur (3).

6. Mémoire flash EEPROM selon la revendication 5, **caractérisée en ce que** lesdits moyens générateurs de courant comprennent une cellule de mémoire de référence (CMR) identique à la cellule de mémoire lue (CM) et ayant une tension de seuil prédéterminée.

7. Mémoire flash EEPROM selon la revendication 5 ou 6, **caractérisée par** l'inclusion d'un second condensateur de découplage (C2) monté entre ladite sortie (20) de la seconde branche de conversion (2) et la seconde entrée du comparateur (3), et par l'inclusion d'un second moyen à transistor (23) monté entre la seconde entrée du comparateur (3) et l'alimentation (Vdd) et activable pour relier électriquement le second condensateur de découplage (C2) à l'alimentation (Vdd).

8. Mémoire flash EEPROM selon la revendication 7, ledit dispositif de mémoire à semi-conducteur comprenant une matrice de cellules de mémoire (CM) placées à l'intersection de lignes (WL) et de colonnes (BL) de la matrice, des moyens (5, 6) de sélection de colonne pour relier électriquement l'une d'un groupe desdites colonnes (BL) à ladite première branche (1) de conversion courant/tension, un moyen (50) de décodage d'adresse pour générer des signaux (YN0-YN7, YM0-YM7) de sélection de colonne pour attaquer lesdits moyens (5, 6) de sélection de colonne et des signaux (WL0, WL1, WLm) de sélection de ligne pour sélectionner l'une desdites lignes (WL) en réponse à des signaux extérieurs d'adresse (A0-An) du dispositif de mémoire, le moyen de décodage d'adresse comprenant des moyens (D, 27, 28) de détection de transition d'adresse pour activer temporairement ledit moyen à transistor (13), en réponse à un changement dans les signaux extérieurs d'adresse (A0-An), pendant une durée prédéterminée entre l'activation des signaux (YN0-YN7, YM0-YM7) de sélection de colonne et l'activation des signaux (WL0, WL1, WLm) de sélection de ligne.

Fig.1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13
VC2
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21
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2
9
V9
C1
V12
12
22
C2
V20
20
V22
14
18
8
10
19
ATD
15
7
YM0
6
YM7
6
VDD
4
4
17
16
YN0
5
5
5
5
CBLR
YN7
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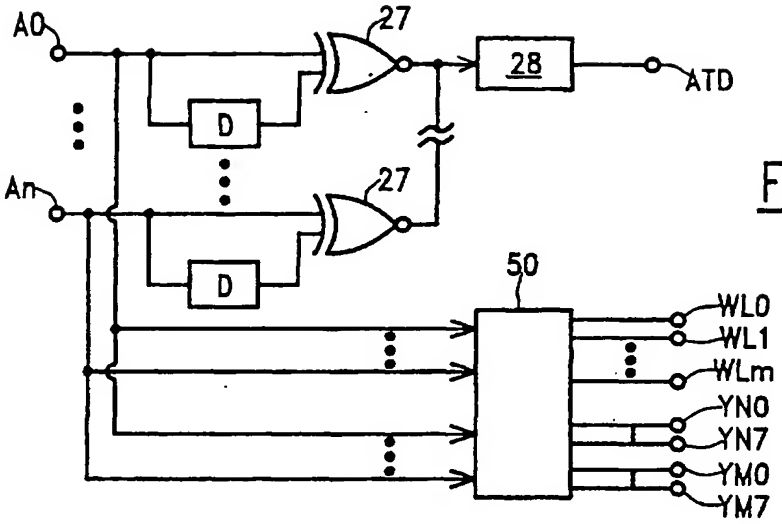


Fig.2

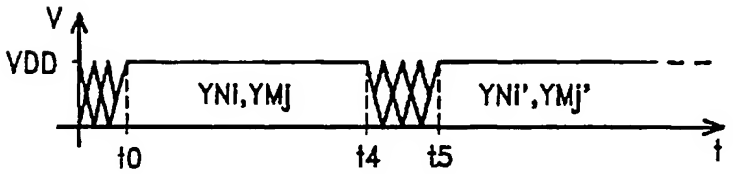


Fig.3A

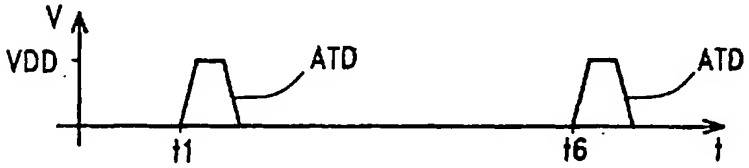


Fig.3B

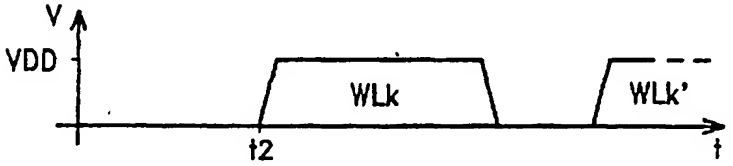


Fig.3C

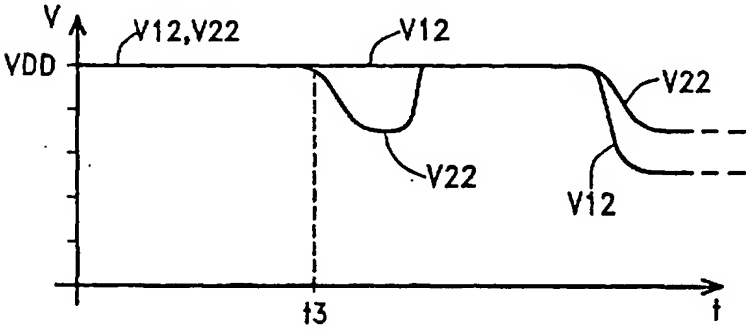
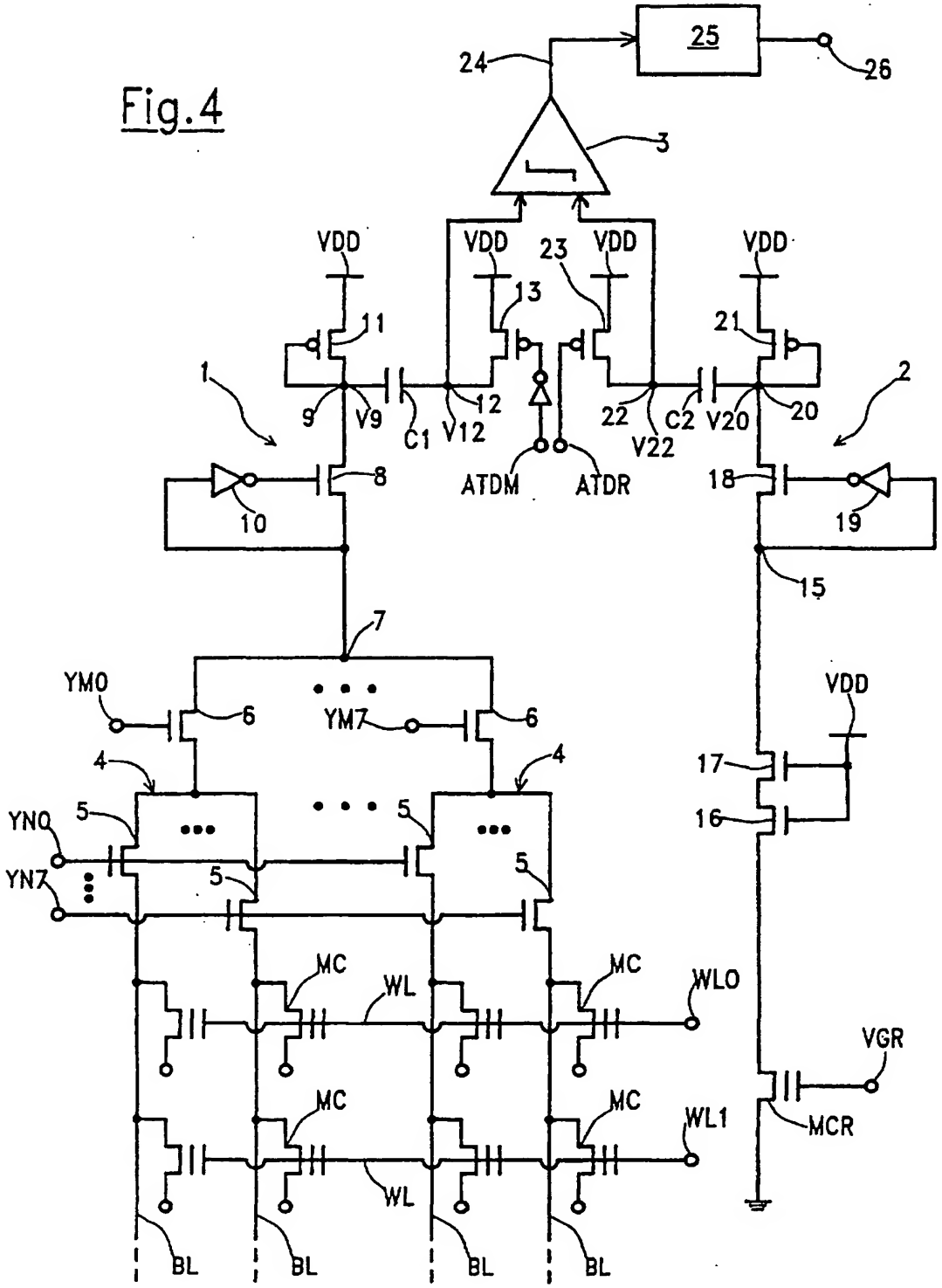


Fig.3D

Fig.4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C2
V20
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V22
ATDM
ATDR
8
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10
19
15
7
YM0
YM7
6
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VDD
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17
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YN0
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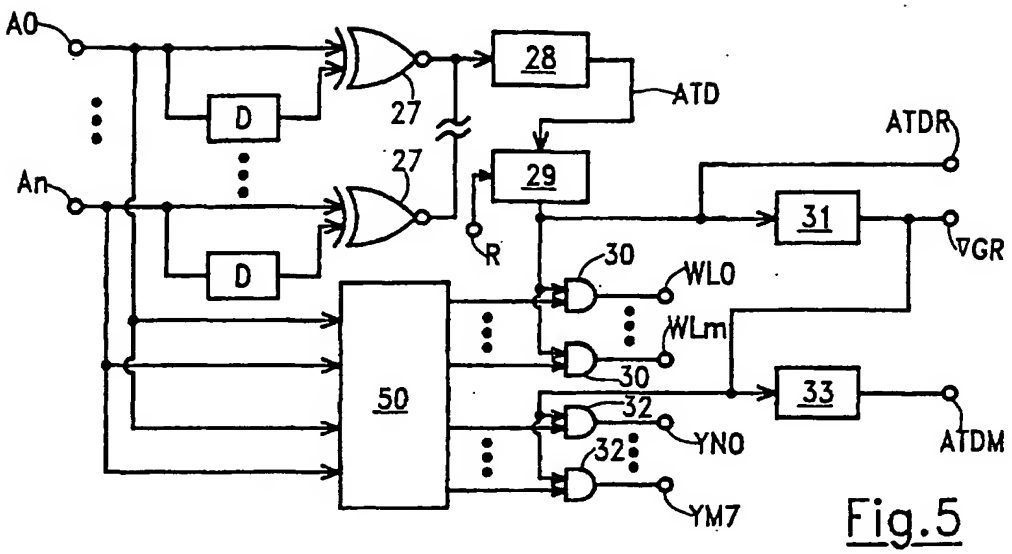

Fig.5

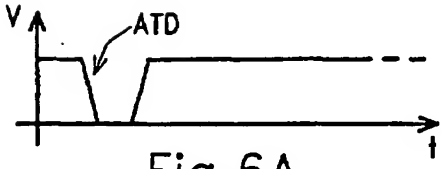

Fig.6A

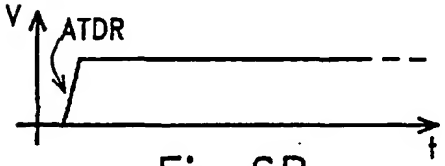

Fig.6B

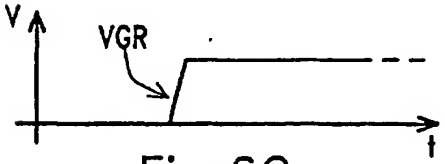

Fig.6C

Fig.6D

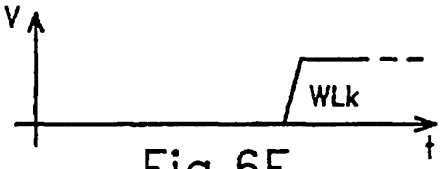

Fig.6E

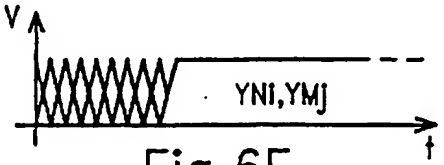

Fig.6F

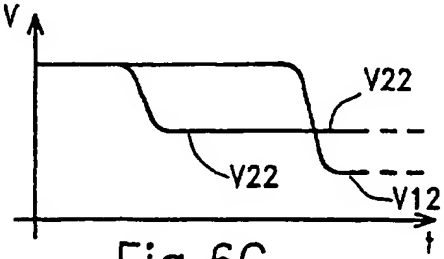

Fig.6G